GlobalFoundries Product/Patent Marking Document

GF Product	US Patents	Title	Issue Date
GaN and CSOI8SW	10,062,748	Segmented guard-ring and chip edge seals	2018-08-28
7HV	8,507,983	High voltage device	2013-08-13
SIGE8HP and SIGE8XP	9,269,666	Methods for selective reverse mask planarization and interconnect structures formed thereby	2016-02-23
130CBIC	9,093,425	Self-aligned liner formed on metal semiconductor alloy contacts	2015-07-28
	8,330,235	Method to reduce mol damage on NiSi	2012-12-11
	11,658,177	Semiconductor device structures with a substrate biasing scheme	2023-05-23
	9,865,546	Contacts to semiconductor substrate and methods of forming same	2018-01-09
	10,707,167	Contacts to semiconductor substrate and methods of forming same	2020-07-07
130BCD	11,380,759	Transistor with embedded isolation layer in bulk substrate	2022-07-05
12LP+	11,557,421	Integrated circuit structure with dielectric material to cover horizontally separated metal layers, and related method	2023-01-17
130BCDlite	10,797,171	Laterally diffused mosfet with locos dot	2020-10-06
9SW	8,283,193	Integrated circuit system with sealring and method of manufacture thereof	2012-10-09
14LPP / 12LP	7,750,418	Introduction of metal impurity to change workfunction of conductive electrodes	2010-07-06
	8,912,603	Semiconductor device with stressed fin sections	2014-12-16
	9,105,643	Bit cell with double patterned metal layer structures	2015-08-11